A core that obtains a fixed-point square root is presented. The algorithm used has been proposed by Li and Chu [1]. Three types of architecture are presented: a low cost iterative version, a fully pipelined version, and a fully combinatorial version. The user can scale the size of the core, choose the precision bits required and select the architecture by simply setting parameters. In order to prove the efficiency of the algorithm, the algorithm is targeted to FPGAs in order to establish a comparison with a core provided by a leading vendor: ALTERA Corporation. The results are very encouraging: the core consumes fewer gates, is faster and has more options than the ALTERA core. The core is described in VHDL, and the results were obtained using the Quartus II 4.2 Web Edition.