Abstract: Using reconfigurable static random access memory (SRAM)-based field-programmable gate arrays (FPGAs) for space-based computation has been a very active area of research for the past decade. Because these commercially available devices are only radiation tolerant in terms of total ionizing dose and single-event latchup, these devices must be qualified for other types of single-event effects to be used in spacecraft. Furthermore, mission requirements often dictate the need to do radiation experiments on the FPGA user circuit. Because both the circuit and the circuit's state are stored in memory that is susceptible to single-event upsets, both could be altered by the harsh space radiation environment. Both the circuit and the circuit's state can be protected by triple-modular redundancy (TMR), but applying TMR to FPGA user designs is often an error-prone process. Faulty application of TMR could cause the FPGA user circuit to output incorrect data. This paper will describe both device-level static testing and user circuit dynamic testing, including a three-tiered methodology for testing FPGA user designs for space readiness.